Claims

[1] A motor driving circuit for driving a motor by driving a first NMOS and a second NMOS coupled in series to the final output stage where a common node of the source of the first NMOS and the drain of the second NMOS serves as the final output, said motor driving circuit comprising:

a first PMOS and a third NMOS having a common node of drains thereof coupled to the gate of the first NMOS;

a second PMOS and a fourth NMOS having a common node of drains thereof coupled to the gate of the third NMOS;

one or more PMOSs having drains coupled to the gate of the third NMOS which are turned on to charge the gate capacity of the third NMOS when the final output is low and are turned off when gate capacity of the third NMOS is charged; and

one or more NMOSs having drains coupled to the gate of the third NMOS which are turned on to discharge the gate capacity of the third NMOS when the final output is high and are turned off when the gate capacity of the third NMOS is discharged, wherein the gate of the first NMOS is coupled to the final output through a clamp circuit and the source of the third NMOS and the gate of the third NMOS through a clamp circuit are coupled to the final output.

[2] A motor driving circuit according to claim 1, characterized in that the clamp circuit is a Zener diode.

[3] A motor driving circuit according to claim 1 or 2, characterized in that the motor driving circuit includes the first NMOS and the second NMOS.

[4] A semiconductor device having the motor driving circuit according to claims 1 or 2.

[5] A motor device including the semiconductor device according to claim 4 and a motor having a coil driven by the semiconductor device.